UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Line 2, please insert

-- FIELD OF THE INVENTION

This invention relates to anti-jitter circuits (AJC) --.

Column 6, line 55 - Column 8, line 56,
Replace the claims in their entirety with the following:

1. **An anti-jitter circuit for reducing time jitter in an input pulse train comprising:**

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage,

a low pass filter coupled to said integrator charge storage means for deriving a mean d.c. voltage of said time varying voltage, and

means for comparing said time varying voltage with said mean d.c. voltage and deriving an output pulse train as a result of the comparison.

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

2. **An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and said low pass filter defines a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage substantially constant.**

3. **An anti-jitter circuit as claimed in claim 2 wherein said discharge device is a current source or a current sink.**

4. **An anti-jitter circuit as claimed in claim 3 wherein said discharge device is a transistor.**

5. **An anti-jitter circuit as claimed in claim 2 wherein said mean d.c. voltage is generated at an output of said negative feedback path and said means for comparing comprises a comparator having a first input coupled to the integrator charge storage means and a second input coupled to said output of the negative feedback path.**

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

6. An anti-jitter circuit as claimed in claim 2 further including a monostable circuit connected to the output of said means for comparing.

7. An anti-jitter circuit as claimed in claim 6 wherein said d.c. voltage is used to control the pulse length of pulses output by the monostable circuit.

8. An anti-jitter circuit as claimed in claim 7 wherein the monostable circuit is a current-controlled monostable circuit and has a control input coupled to an output of said negative feedback path by a current mirror matched to said discharge device.

9. An anti-jitter circuit as claimed in claim 8 wherein said discharge device and said current mirror are matched transistors.

10. An anti-jitter circuit as claimed in claim 6 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage crosses the mean d.c. voltage.

11. An anti-jitter circuit as claimed in claim 2 including means providing a low impedance path between the input and the output of the negative feedback path.

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

12. An anti-jitter circuit as claimed in claim 11 wherein said low impedance path is formed by diodes connected back-to-back.

13. An anti-jitter circuit as claimed in claim 1 wherein the low pass filter comprises the combination of a resistor and a capacitor.

14. An anti-jitter circuit as claimed in claim 1, wherein said charging means comprises a first charging means and a second charging means for deriving the charge packets respectively from the rising and falling edges of the input pulse train, said first and second charging means being effective as a frequency doubling means.

15. An anti-jitter circuit as claim in claim 1 further including means for maintaining the charge value of the charge packets substantially constant.

16. An anti-jitter circuit as claimed in claim 15 wherein said means for maintaining comprises a further transistor coupled between said charging means and said integrator charge storage means.

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

17. **An anti-jitter circuit as claimed in claim 16 wherein said further transistor is arranged to operate in grounded base mode.**

18. **An anti-jitter circuit as claimed in claim 17 including averaging means connected to the base of the further transistor.**

19. **An anti-jitter circuit as claimed in claim 16 wherein said discharging means includes a first field effect transistor operative as a discharge device and said further transistor is a second field effective transistor, and the gate of the first field effect transistor is connected to the gate of the second field effect transistor.**

20. **An anti-jitter circuit as claimed in claim 1 wherein said charging means is a charge pump.**

21. **An anti-jitter circuit for reducing time jitter in an input pulse train comprising:**

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means, said discharging means comprising a discharge device having a control input,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage, and

means for comparing said time varying voltage with a mean d.c. voltage and deriving an output pulse train as a result of the comparison, said means for comparing comprising a low pass filter coupled to said integrator charge storage means for deriving said mean d.c. voltage of said time varying voltage, said low pass filter comprising a resistor and a capacitor connected in series across said integrator charge storage means, said low pass filter defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage substantially constant, aid means for comparing further comprising inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c. voltage as a switching level of said inverted gate means.

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

22. **An anti-jitter circuit as claimed in claim 21 wherein said further negative feedback path is connected between said output of said inverted gate means and said control input of said discharge device.**

23. **An anti-jitter circuit as claimed in claim 22 wherein said further negative feedback path comprises a further low pass filter.**

24. **An anti-jitter circuit as claimed in claim 23 wherein said further low pass filter comprises the combination of a resistor and a capacitor.**

25. **An anti-jitter circuit as claimed in claim 21 wherein said further negative feedback path comprises a further low pass filter.**

26. **An anti-jitter circuit as claimed in claim 25 wherein said further low pass filter comprises the combination of a resistor and a capacitor.**

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

27. **An anti-jitter circuit for reducing time jitter in an input pulse train comprising:**

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means, said discharging means comprising a discharge device having a control input,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage, and

means for comparing said time varying voltage with a mean d.c. voltage and deriving an output pulse train as a result of the comparison, said means for comparing comprising a low pass filter coupled to said integrator charge storage means for deriving said mean d.c. voltage of said time varying voltage, said low pass filter comprising a resistor and a capacitor connected in series across said integrator charge storage means, said low pass filter defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage substantially constant, said means for comparing further comprising, inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c. voltage as a switching level of said inverted gate means.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1
DATED : September 14, 2004
INVENTOR(S) : Underhill

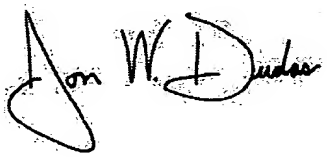
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55 - Column 8, line 56 (cont'd),

28. An anti-jitter circuit as claimed in claim 27 wherein said voltage source is connected between said output of said inverted gate means and said control input of said discharge device.

Signed and Sealed this

Twenty-third Day of August, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office